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			AbstractPlus Full Text: PDF(1434 KB) IEEE JNI.
			 43 Gb/s full-rate-clock 16:1 multiplexer and 1:16 demultiplexer with SFI-5 interface BiCMOS technology Koyama, A.; Harada, T.; Yamashita, H.; Takeyari, R.; Shiramizu, N.; Ishikawa, K.; Ito, Yamashita, T.; Yabuki, S.; Ando, H.; Aida, T.; Watanabe, K.; Ohhata, K.; Takeuchi, S. Yoshioka, H.; Kubota, A.; Takahashi, T.; Nii, H.; Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE 2003 Page(s):232 - 490 vol.1
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Day: Sunday Date: 7/17/2005

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Application Number Information

Application Number: 09/988896

Assignments

Filing or 371(c) Date: 11/19/2001

Effective Date: 11/19/2001

Application Received: 11/21/2001

Pat. Num./Pub. Num: /20030095575

Issue Date: 00/00/0000

Date of Abandonment: 00/00/0000

Confirmation Number: 9182

Unmatched Petition: NO

Interference Number:

Lost Case: NO

Group Art Unit: 2667

L&R Code: Secrecy Code:1

Class/Subclass: 370/516.000

Attorney Docket Number: 021067-000200US Third Level Review: NO

Secrecy Order: NO Status Date: 03/17/2002 Status: 30 /DOCKETED NEW CASE - READY FOR EXAMINATION

Examiner Number: 76906 / JONES, PRENELL

IFW IMAGE

Oral Hearing: NO

Title of Invention: METHOD AND CIRCUIT FOR DE-SKEWING DATA IN A

COMMUNICATION SYSTEM

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•	SPT; PLUR=YES; OP=ADJ		
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<u>L28</u>	L26 and de-skewing	0	<u>L28</u>

<u>L27</u>	L26 and de-skew	0	<u>L27</u>
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<u>L11</u>	L6 and first near chip and second near chip	21	<u>L11</u>
<u>L10</u>	L9 and early and late	4	<u>L10</u>
<u>L9</u>	L8 and bits	10	<u>L9</u>
<u>L8</u>	L6 and training near sequence	10	<u>L8</u>
<u>L7</u>	L6 and sequence and training near bits	2	<u>L7</u>
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<u>L5</u>	SONET and training near sequence and training near bit	2	<u>L5</u>
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<u>L3</u>	late near skew and early near skew	2	<u>L3</u>
DB=U	SPT; PLUR=YES; OP=ADJ		
<u>L2</u>	late near skew and early near skew	0.	<u>L2</u>
L1	late near scew and early near scew	0	L1

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